WHAT IS CLAIMED IS:

1. An event based semiconductor test system for testing semiconductor devices and displaying test parameters and test results, comprising:

means for generating a test pattern and applying the test pattern to a semiconductor device under test;

means for evaluating a response output of the semiconductor device under test and collecting test result data; and

a host computer for controlling an overall operation of the event based test system and for displaying test parameters and the test result data;

wherein the host computer displays a device characterization map in which the test parameters and the test result data are illustrated in a multi-dimensional manner on X, Y and Z axes.

2. An event based semiconductor test system as defined in Claim 1, wherein the characterization map includes a checkerboard map which shows the test results configured by pins versus time, a shmoo plot which shows pass-fail boundary points relative to predetermined parameters with respect to a single device under test, a composite map which shows a composite data of shmoo plots of a plurality of devices under test, a margin map which shows pass/fail ranges for individual pins or pin groups corresponding with one or more events, and a waveform display which shows a test pattern to be applied to the device under test based on the event data from the event memory.

3. An event based semiconductor test system as defined in Claim 1, wherein the characterization map includes a checkerboard map which shows the test results configured by pins versus time wherein a time scale of the

checkerboard map is expanded or compressed by a timing scaling function of the event based test system.

4. An event based semiconductor test system as defined in Claim 1, wherein the characterization map includes a shmoo plot which shows pass-fail boundary points relative to predetermined parameters with respect to a single device under test and a composite map which shows a composite data of shmoo plots of a plurality of devices under test wherein a time scale of the shmoo plot or composite map is expanded or compressed by a timing scaling function of the event based test system.

5. An event based semiconductor test system as defined in Claim 1, wherein the characterization map includes a margin map which shows pass/fail ranges for individual pins or pin groups corresponding with one or more events wherein a position of an edge of the event is changed by a timing offset function of the event based test system.

6. An event based semiconductor test system as defined in Claim 1, wherein the characterization map displays the waveforms of the test pattern to be applied to the device under test based on the event data from the event memory, wherein the characterization map shows an overall illustration of the test pattern, an enlarged view of a part of the test pattern, timing changes in each event in the test pattern, and/or offset addition or removal from the test pattern.